Yash Patel

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EDUCATION

University of New Hampshire — Durham, New Hampshire
Bachelor of Science in Computer Engineering — May 2026

- **Courses:** FPGA Design, Embedded Systems Design, Digital Systems Design, Electronic Circuit Design, Communication Systems Design, Operating Systems, Computer Architecture

EXPERIENCE

University of New Hampshire — InterOperability Labs — Durham, New Hampshire
Senior Test Engineer — Apr 2025 - Present

- **2.5/5/10GBASE-T1 Ethernet Decoder:** Engineered the first commercially available multi-gigabit Single-Pair Ethernet decoder and analysis tool in Rust, recovering PAM-4 symbols, decoding infofields, and extracting data from RS-FEC protected frames from raw oscilloscope captures at 60x the throughput of the legacy MATLAB based system.
- **Clause 149 PHY Validation**: Validated MultiGBASE-T1 PHY-Control (IEEE 802.3 Clause 149) implementations, analyzing link-training state machines, NRZ/PAM-4 signal integrity, and RS-FEC performance using Rust, Python, and Verilog tooling.
- **Standards Development:** Drove technical revisions to OPEN Alliance conformance test plans progressing toward ISO 21111-6, including removing tests whose requirements were unachievable.
- **AXI4 Manager RTL:** Designed a multi-input AXI4 write manager in Verilog, verified via Python cocotb with 96% functional coverage of the write-channel protocol.

Junior Test Engineer — Jan 2024 - Apr 2025

- **MDIO Transmitter RTL:** Architected an IEEE 802.3 Clause 22/45 MDIO transmitter in Verilog for a custom FPGA test automation framework, integrated into commercial-grade hardware validation suites.
- **100BASE-T1 Conformance Automation**: Built a 100BASE-T1 PHY Control and PCS automation tool in Rust and MATLAB that ingests oscilloscope captures over SCPI and programmatically determines pass/fail, removing manual analysis from the test loop.
- **Technical Lead, Vendor Test Engagements:** Led end-to-end testing for 20+ concurrent vendor engagements, delivering weekly reports and root-cause analysis of Single-Pair Ethernet PHY behavior.

INDUSTRY CONTRIBUTIONS

- **Acknowledged Contributor, OPEN Alliance IEEE 100BASE-T1 Test Suite V1.4:** Recognized in the specification acknowledgments for driving major technical revisions, including optimizing test coverage, deprecating obsolete tests, and refining functional requirements for conformance testing.

SKILLS

- **Languages & HDL:** Rust, C, Verilog, Python, MATLAB, Bash, Lua
- **Protocols & Signaling:** IEEE 802.3 (100BASE-T1, MultiGBASE-T1), MDIO, AXI4, PAM-4, I2C, SPI, UART, CAN
- **Tools:** cocotb, Vivado, Quartus, LabVIEW, Oscilloscopes, Logic Analyzers, Wireshark, Git
- **Hardware & Platforms:** Xilinx FPGA, Altera FPGA, STM32, ESP32, MSP430, PicoScope, Linux

PROJECTS

Smart Adaptive Audio Equalizer Headset
Senior Design Project

- **Role and Architecture:** DSP and hardware lead on a 3-person team designing an ESP32-based adaptive headset combining active cancellation of ambient and internal biological noise.
- **Personalized DSP Calibration:** Led development of a 60-second automated hearing test that generates a per-user audio profile, applied as real-time equalization to playback.
- **Feedforward/Feedback ANC Signal Path:** Led design of a dual-microphone feedforward/feedback signal path on the ESP32, suppressing urban ambient noise and internal interference such as blood-flow sounds.